Course Structure & Syllabus
of
M. Tech. Programme
in
Electronics & Telecommunication Engineering
with Specialisation
VLSI SIGNAL PROCESSING
Academic Year – 2016-17

VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY, ODISHA
Burla, Sambalpur-68018, Odisha
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DEPARTMENT VISION:

Developing new ideas in the field of communication to enable students to learn new technologies, assimilate appropriate skills and deliver meaningful services to the global society and improve the quality of life by training them with strength of character, leadership and self-attainment.

DEPARTMENT MISSION:

- Imparting futuristic technical education to the students.
- Promoting active role of Industry in student curriculum, projects, R&D and placements. Organizing collaborative academic and non-academic programmes with institutions of national and international repute for all round development of students.
- Organizing National and International seminars and symposium for exchange of innovation, technology and information.
- Expanding curricula to cater to demands of higher studies in internationally acclaimed institutes. Preparing students for promoting self-employment.
- Develop the department as a centre of excellence in the field of VLSI and communication technology by promoting research, consultancy and innovation.

VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY, ODISHA, BURLA
DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING
Course Structure & Curriculum for M.Tech in *VLSI SIGNAL PROCESSING*

Subject Code	Subjects	L	T	P	C
FIRST SEMESTER					
	Analog VLSI Design	3	1	0	4
	Digital VLSI Design	3	1	0	4
	VLSI Technology	3	1	0	4
	Elective-I	3	1	0	4
	Elective-II	3	1	0	4
	VLSI Design Laboratory-I	0	0	3	2
	VLSI Technology Laboratory	0	0	3	2
	Seminar-I	0	0	3	2
	Comprehensive Viva-Voce-I				2
	Total Credits->	15	5	9	28
SECOND SEMESTER					
	HDL & High Level VLSI Design	3	1	0	4
	VLSI Signal Processing	3	1	0	4
	VLSI Testing	3	1	0	4
	Elective-III	3	1	0	4
	Elective-IV	3	1	0	4
	VLSI Design Laboratory-II	0	0	3	2
	Advanced Simulation Laboratory	0	0	3	2
	Seminar-II	0	0	3	2
	Comprehensive Viva-Voce-II				2
	Total Credits->	15	5	9	28
THIRD SEMESTER					
	Dissertation Interim Evaluation				10
	Comprehensive Viva-Voce				3
	Seminar on Dissertation				5
				Total Credits->	15
FOURTH SEMESTER					
	Dissertation Open Defense				5
	Dissertation Final Evaluation				20
				Total Credits->	25
				Grand Total Credits->	96

ELECTIVE-I/ ELECTIVE-II	**ELECTIVE-III/ ELECTIVE-IV**
Advanced Signal Processing	Digital Signal Processor Architectures
Computational Techniques in Microelectronics	Design with ASICS
FPGA Based DSP Design	MEMs & IC Design
Advanced Computer Architecture	Physical Design Automation
Semiconductor Device Modeling	CMOS RF Circuit Design
RF Solid State Device	Embedded System Design
TCAD Modeling	Low Power VLSI Design
VLSI Algorithms	System on Chip (SoC) Design

ANALOG VLSI DESIGN :(3-1-0) Credit: 4

COURSE OBJECTIVE:

1. To understand the static, small signal and large signal modelling of MOS Transistor.
2. To understand the operation of different MOS Amplifier and Operational Amplifier.
3. To understand the operation of different MOS current mirror circuits and comparators.

MODULE-I **10 hours**

MOS Device and Modeling: The MOS Transistor, Passive Components- Capacitors and Resistors, Integrated Circuit Layout, CMOS Device Modeling- Simple MOS Large Signal Model, Other MOS Large Signal Model Parameters, Small Signal Model of the MOS Transistor, Computer Simulator Models, Subthreshold MOS Model.

MODULE-II **10 hours**

Analog CMOS Sub Circuits: MOS Switch, MOS Diode/Active Resistor, MOS Current Sinks and Sources, Current Mirrors- Current Mirror with Beta Helper, Cascode Current Mirror and Wilson Current Mirror, Voltage and Current References, Bandgap Reference, CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers.

MODULE-III **10 hours**

CMOS Operational Amplifiers: Design of Op-Amps, Compensation of OP-Amps, Design of a Two-Stage OP-Amp, Power Supply Rejection Ratio of Two Stage Op-Amp.

MODULE-IV **10 hours**

Comparators: Characterization of a Comparator, Two Stage Open Loop Comparators, Discrete Time Comparators. Other Open Loop Comparators, Improving the Performance of Open Loop Comparators.

Text Books

1. Philip.E. Allen and Douglas.R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press, Indian3rd Edition, 2012.
2. Paul.R. Gray, Paul.J. Hurst, S.H. Lewis and R.G.Meyer, *Analysis and Design of Analog Integrated Circuits*, Wiley India, Fifth Edition, 2010

Reference Books

1. R.J. Baker, H. W. Li, D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, PHI, 2002
2. D.A. Johns and K. Martin, *Analog Integrated Circuit Design*; Wiley Student Edition, 2013
3. B. Razavi; *Design of Analog CMOS Integrated Circuits*, Tata McGraw-Hill, 2002

COURSE OUTCOME:

1. Ability of extract the MOS amplification parameters.
2. Design improved CMOS amplifiers and Operational Amplifiers.
3. Design improved MOS current mirror circuits and comparators.

DIGITAL VLSI DESIGN: (3-1-0) Credit: 4

COURSE OBJECTIVE:

1. Study the characteristics of MOS as an Inverter.
2. Study the behavior of MOS in Combinational circuits.
3. Study the behavior of MOS in sequential circuits.

MODULE –I **10 hours**

Introduction to MOSFETs: MOS Inverter, Static and Switching Characteristics, Voltage Transfer characteristics, Noise Margin, Regenerative Property, Power and Energy Consumption, Stick/Layout Diagrams; Issues of Scaling.

MODULE –II **10 hours**

Combinational MOS Logic Circuits: Pass Transistors, Transmission Gates, Primitive Logic Gates; Complex Logic Circuits, Sequential MOS Logic Circuits: Latches and Flip-flops, Dynamic Logic Circuits; Clocking Issues, Rules for Clocking, Performance Analysis, Logical effort.

MODULE –III **10 hours**

CMOS Subsystem Design; Data Path and Array Subsystems: Addition, Subtraction, Comparators, Counters, Coding, Multiplication and Division.

MODULE –IV **10 hours**

SRAM, DRAM, ROM, Serial Access Memory, Content Addressable Memory, Field Programmable Gate Array.

Text Books

1. Rabey J.M, A. Chandrakasan, and B.Nicolic, Digital Integrated Circuits: A design Perspective, Second Edition, Pearson/PH, 2003 (Cheap Edition).

2.Hodges, David A, Analysis and Design Of Digital Integrated Circuits, In Deep Submicron Technology , Tata McGraw-Hill Education, 2005.

Reference Books

1. Kang, Sung-Mo, and Yusuf Leblebici. CMOS Digital Integrated Circuits, Tata McGraw-Hill Education, 2003.

2. J.P Uyemura, Introduction to VLSI Circuits and Systems, Wiley, 2001

3. R. L. Geiger, P.E. Allen and N.R. Strader, VLSI Techniques for Analog and Digital Circuits, McGraw-Hill, 1990

3. DebaprasadDas , VLSI Design, Oxford Publication.

COURSE OUTCOME:

1. Ability of extract the MOS switching parameters.
2. Efficient design of combinational circuits.
3. Efficient design of sequential circuits.

VLSI TECHNOLOGY :(3-1-0) Credit: 4

COURSE OBJECTIVE:

1. Study of semiconductor crystal structure and properties.
2. Learning the steps followed in fabrication process.
3. Study of electrical testing, packaging and yielding.

MODULE-I 10 hours

Overview of MOS Transistor.Silicon Wafer Preparation for MOS Transistor:Silicon crystal structure,Defects in silicon crystal,Single crystal silicon-Wafer fabrication for MOS transistor application,Fabrication of silicon wafer,Defects and impurities in silicon wafer.

MOS Transistor process flow:MOS Transistor fabrication,device isolation,CMOS fabrication.

MODULE-II 10 hours

Oxidation :Growth mechanism and kinetic oxidation, oxidation techniques and systems, oxide properties, oxide induced defects, characterization of oxide films, Use of thermal oxide and CVD oxide, growth and properties of dry and wet oxide, dopant distribution, oxide quality.

Diffusion:Introduction,Diffusion Equipment and process,Diffusion Models,Modification of Flick's law,Oxidation Effects on Diffusion.

MODULE-III 10 hours

Ion implantation – Range theory, Equipments,Ion implantation parameter affecting the Dose and Uniformity,Implant Damage and annealing,

Etching: Wet chemical etching, Dry etching.

Lithography:Introduction, Photolithographic Process, Photo resist,Non-Photo resist,Light Source and Optical Exposure Systems,Pattern Transferring Techniques and Mask Aligner,Optical Lithography ,Electron Lithography,X-Ray Lithography,Ion Lithography.

MODULE-IV 10 hours

Dielectric and Polysilicon film deposition:Introduction,Deposition process,Chemical Vapor deposition,Physical Vapor deposition,polysilicon,Silicon Dioxide,Silicon Nitride,Plasma Assisted Deposition.

Metallization - Different types of metallization, uses & desired properties.

IC Manufacturing: Electrical testing, Packaging,yield.

Text Book

1)Gary S. May, Simon M. Sze, Fundamentals of Semiconductor Fabrication, John Wiley Inc.,2004

2) The Science and Engineering of Microelectronic Fabrication, Stephen Cambell, Oxford University Press, 2001.

Referance Books

1) Gauranga Bose, IC Fabrication Technology, McGraw hill Education
2) J. D. Plummer, M. D. Deal and P. B. Griffin, Silicon VLSI Technology Fundamentals, Practice and Models, Prentice Hall, 2000

COURSE OUTCOME:

1. Can design improved compound semiconductors.
2. Acquainted with recent technology.

ELECTIVE – I/II

ADVANCED SIGNAL PROCESSING: (3-1-0)Credit: 4

COURSE OBJECTIVE:

1. Study about the multirate signal processing.
2. study of linear prediction and power spectrum estimation of signals.
3. Study of adaptive signal processing.

MODULE-I **10 hours**

Multirate Digital Signal Processing: Introduction, Decimation by a Factor D, Interpolation by a Factor I, Sampling Rate Conversion by Rational Factor I/D, Filter Design and Implementation for Sampling-Rate, Multistage Implementation of Sampling Rate Conversion, Sampling Rate Conversion of Band Pass Signal, Application of Multi Rate Signal Processing: Design of Phase Shifters, Implementation of Narrowband Low Pass Filters. Implementation of Digital Filter Banks. Filter Bank and Sub band Filter Applications.

MODULE-II **10 hours**

Linear Prediction and Optimum Linear Filters: Innovations Representation of a Stationary Random Process, Forward and Backward Linear Prediction, Solution of the Normal Equations, Properties of the Linear Prediction-Error Filters, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filter for Filtering and Prediction: FIR Wiener Filter, Orthogonality Principle in Linear Mean-Square Estimation.

MODULE-III **10 hours**

Power Spectrum Estimation: Estimation of Spectra from Finite-Duration Observation of Signals, Non Parametric Method for Power Spectrum Estimation: Bartlett Method, Blackman and Turkey Method, Parametric Method for Power Estimation: Yuke-Walker Method, Burg Method, MA Model and ARMA Model. Higher Order Statics (HOS): Moments, Cumulants, Blind Parameters and Order Estimation of MA & ARMA Systems-Application of Higher Order Statistics.

MODULE-IV **10 hours**

Adaptive Signal Processing: Least Mean Square Algorithm, Recursive Least Square Algorithm, Variants of LMS Algorithm: SK-LMS, N-LMS, FX-LMS. Adaptive FIR & IIR Filters, Application of Adaptive Signal Processing: System Identification, Channel Equalization, Adaptive Noise Cancellation, Adaptive Line Enhancer.

Text Books

1. J.G. Proakis and D.G. Manolakis, *Digital Signal Processing*, Third Edition, Prentice Hall
2. B. Widrow and Stern, *Adaptive Signal Processing*
3. Haykins, *Adaptive Filter*, PHI

COURSE OUTCOME:

1. Multistage implementation of sampling rate conversion.
2. Implementation adaptive algorithms in filter design.
3. Solve real time problems like system identification, Noise cancellation etc.

COMPUTATIONAL TECHNIQUES IN MICRO-ELECTRONICS :(3-1-0) Credit: 4

COURSE OBJECTIVE:

1. Study of Linear and Non-Linear Circuit Simulation Techniques
2. Study of Symbolic Analysis and Synthesis of Analog ICs.
3. Study of physical design algorithms.

MODULE-I **10 hours**

Linear and Non-Linear Circuit Simulation Techniques- Algorithms and Computational Methods; Transient Analysis; Frequency Domain Analysis.

MODULE-II **10 hours**

Moment Methods; Sensitivity Analysis, Timing Simulation. Numerical Solution of Differential Equations- FEM, FVM and FDM, Grid Generation, Error Estimates, Transient and Small Signal Solutions, Applications to Device and Process Simulation.

MODULE-III 10 hours

Introduction to VHDL Modeling. Layout Algorithms, Yield Estimation Algorithms. Symbolic Analysis and Synthesis of Analog ICs.

MODULE-IV **10 hours**

Introduction to Physical Design, Part Training Algorithms, Algorithms for Placement and Floor Planning, Global Routing And Detailed Routing.

Text Book*s*:

1. L.O.CHUA AND P.M.LIN "*Computer Aided Analysis of Electronics Circuits: Algorithms and Computational Techniques*"., Prentice –Hall 1975.
2. L.PALLAGE, R.ROHRER ANDC.VISWESWARAIAH, "*Electronics Circuits and Simulation Methods"*, Mc. Graw Hall, 1995.

Referance Books:

1., NAVEED SHEWANI, "*Algorithms for VLSI Physical Design Automation*", Kluwer Academic, 1993

COURSE OUTCOME:

1. Implementation of computational techniques in physical design.
2. Able to propose new algorithms.

FPGA BASED DSP DESIGN :(3-1-0) Credit: 4

COURSE OBJECTIVE:

1. Study of multitone modulation.
2. Brief idea about software radio.
3. Study of Speech Coding Using Linear Prediction.

MODULE-I **10 hours**

Multirate Signal Processing- Decimation and Interpolation, Spectrum of Decimated and Interpolated Signals, Polyphase Decomposition of FIR Filters and Its Applications to Multirate DSP. Sampling Rate Converters, Sub-Band Encoder. Filter Banks-Uniform Filter Bank. Direct and DFT Approaches.

MODULE -II **10 hours**

Introduction to ADSL Modem, Discrete Multitone Modulation and it's Realization Using DFT. QMF. Short Time Fourier Transform Computation of DWT Using Filter Banks. Implementation and Verification on FPGAs. DDFS- ROM LUT Approach. Spurious Signals Jitter. Computation of Special Functions Using CORDIC.Vector and Rotation Mode of CORDIC. CORDIC Architectures. Implementation and Verification on FPGAs.

MODULE -III **10 hours**

Block Diagram of a Software Radio. Digital Down Converters and Demodulators. Universal Modulator and Demodulator Using CORDIC. Incoherent Demodulation - Digital Approach for I and Q Generation, Special Sampling Schemes. CIC Filters. Residue Number System and High Speed Filters Using RNS. Down Conversion Using Discrete Hilbert Transform. Under sampling Receivers, Coherent Demodulation Schemes.

MODULE -IV **10 hours**

Speech Coding- Speech Apparatus. Models of Vocal Tract. Speech Coding Using Linear Prediction. CELP Coder. An Overview of Waveform Coding. Vocoders. Vocoder Attributes. Block Diagrams of Encoders and Decoders of G723.1, G726, G727, G728 and G729.

Text Books

1. J. H. Reed, *Software Radio*, Pearson, 2002.
2. U. Meyer – Baese, *Digital Signal Processing with FPGAs*, Springer, 2004

Reference Books

1. Tsui, *Digital Techniques for Wideband receivers*, Artech House, 2001.
2. S. K. Mitra, *Digital Signal processing*, McGrawHill, 1998

COURSE OUTCOME:

1. Design of modem.
2. Design of high speed filters using redundant number system.
3. Use of multirate processing.

ADVANCED COMPUTER ARCHITECTURE (3-1-0) Cr.-4

COURSE OBJECTIVE:

1. Study of parallel processing and program flow control in a processor.
2. Study of multiprocessor and multicomputer.
3. To be acquainted with memory organization of processors.

MODULE-I (10 lectures) 10 hours

Parallel Processing**:** Definition, Theory of Parallelism. Parallel Computer Models,Parallelism in Uni-processor computers, Implicit Parallelism vs. explicit parallelism,Levels of parallelism.Soft ware Parallelism, Hardware Parallelism.Conditions of Parallelism: Data and Resource Dependencies, Control Dependence,Resource dependence, Berrnstein's condition, Hardware and software parallelism, Flowdependence, Anti dependence, output dependence, I/O dependence, unknowndependence.

MODULE-II (10 lectures)10 hours

Program flow Mechanism: Control flow versus data flow, Demand-driven mechanism,Comparison of flow mechanisms, Dataflow computer Architecture, Static dataflow anddynamic dataflow computer, Communication Latency, grain packing and scheduling inparallel programming environment, program partitioning, fine grain program, coarsegrain program graph.

MODULE-III (10 lectures) 10 hours

Parallel Interconnection Systems: Static and Dynamic Networks, Linear Array, Ring,Star, Tree, Mesh, Systolic Array, Chordal ring, Completely connected network, Cubeconnected cycles, Torus, K-ary-n cube, Barrel shifter, single stage interconnectionnetwork, Multistage Interconnection Networks, Control Structure, Node degree,diameter, Bisection width, symmetric, functionality, Network Latency, Bandwidth,Scalability, Data routing functions:- Permutation, Perfect shuffle exchange, HypercubeRouting function.

Pipelining: Linear pipe line processor, Asynchronous and Synchronous models, speedup, Efficiency, Throughput, Non linear pipe line processor, Instruction pipeline, pipeline hazards and Arithmetic pipeline.

MODULE-IV (10 lectures) 10 hours

Multiprocessor and multicomputers: Hierarchical bus system, crossbar and multi portmemory, cross point switch, Flynn's classification: SISD, SIMD, MISD, MIMD,message passing, Loosely coupled and tightly coupled system.Vector processor, memory hierarchy, CISC scalar processor, RISC scalar processor, Caccessand S-access memory organization. Basic ideas on parallel algorithm, SIMDalgorithm for matrix multiplication.Fault-tolerance and reliability, Availability, System Performance attributes of parallelComputers.

Text Books

1. Advanced Computer Architecture, by Kai Hwang Mc Graw Hill.
2. Introduction to Parallel Computing, 2nd Edition, Pearson Education by Ananth Grama, Anshul Gupta, George Karypis, Vipin Kumar.

Referance Books

1. Computer Architecture – A quantitative approach By J.L Hennessy and D.A.Patterson (Morgan)
2. Computer Architecture and Parallel Processing, by K.Hwang and F.A. Briggs. Mc Graw Hill, International

COURSE OUTCOME:

1. They can apply new datapath algorithms to implement a processor more efficiently.
2. They can measure the fault tolerance and reliability of a processor.

SEMICONDUCTOR DEVICE MODELING :(3-1-0) Credit: 4

COURSE OBJECTIVE:

1.To understand the device parameters and characteristics and their implementation in SPICE2.
2. Modelling of diode, bjt and mos transistor.
3. Understand the effect of noise and distortion on device modelling.

MODULE-I10 hours

PN Junction Diode and Schottky Diode: DC Current Voltage Circuits, Static Model, Large Signal Model, Small signal Model, Schottky Diode and its Implementation in SPICE 2, Temperature and Area Effect on the Diode Model Parameters, SPICE3, HSPICE & PSPICE Models.

MODULE-II 10 hours

BJT: Transistor Conversion and Symbols, Ebers-Moll Static, Large Signal and Small Signal Models, Gummel-Poon Static, Large Signal Models, Temperature and Area Effect on the BJT Parameters, Power BJT Models, SPICE3, HSPICE & PSPICE Models

JFET: Static Model, Large Signal Model, Small signal Model and its Implementation in SPICE 2, Temperature and Area Effect on the JFET Model Parameters, SPICE3, HSPICE & PSPICE Models.

MODULE-III 10 hours

Metal Oxide Semiconductor Transistor (MOST): Structure and Operating Regions of the MOST, Level-1 and Level-2 Static Models, Level-1 and Level-2 Large-Signal Models, Comment on the Three Models, The Effect of Series Resistance, Small-Signal Models, The Effect of Temperature on the MOST Model Parameters, BSIM1 & BSIM2 Models, SPICE3, HSPICE & PSPICE Models.

MODULE-IV 10 hours

Noise and Distortion: Noise, Distortion in MOSEFT, ISFET, THYRISTOR.

Text Book

1. G. Massobrio and P.Antognetti, *Semiconductor Device Modeling by SPICE,* Second Edition, McGraw Hill, 1993

Reference Book

1. N. Dasgupta and A. Dasgupta, *Semiconductor Device Modeling,* PHI Publication

COURSE OUTCOME:

1. Ability to model a complex circuit.
2. Ability to implement a circuit in PSPICE.

RF SOLID STATE DEVICE (3-1-0)

COURSE OBJECTIVE:

1. Carrier transport phenomena in semiconductor.
2. Study of microwave devices.
3. Study of transfer electron devices.

MODULE-I **08hours**

Energy Bands & Current Carriers in Semiconductors, Intrinsic & Extrinsic Semiconductor, Junctions, Carrier
Process, Drift-Diffusion, Generation-Recombination

MODULE-II **12hours**

Microwave Transistor, Tunnel Diode, Microwave Field Effect Transistor

MODULE-III **12hours**

Transferred Electron Devices, Avalanche Transit Time Devices

MODULE-IV **08hours**

Optoelectronics, LED, Laser, Photo-detector, Solar Cell

Text Books

1. Semiconductor Devices, By Kanaan Kano, Pearson (Chapters: 2, 3, 4, 14)
2. Solid State Electronic Devices, By B G Streetman & S Banerjee , Pearson (Chapters: 3, 4, 5, 8)
3. Semiconductor Physics & Devices, By D A Neamen, Tata Mc Graw Hill (Chapters: 4, 5, 6, 14)
4. Microwave Devices & Circuits, By S Y Liao, Pearson (Chapter: 5, 6, 7, 8)

Referance Book

1. Microwave Semiconductor Devices and their applications, By Watson ,McGraw Hill
2. Microwave Semiconductors, By H.V Shurmer, Wien Oldenbourg

COURSE OUTCOME:

1. Students can conceptualize various semiconductor physics.
2. They can design various types of RF Solid State Device.
3. They will be also conversant with various optical devices.

TCAD MODELING

COURSE OBJECTIVE:

1. Study of different types of TCADs.
2. Study of different characterization tools.
3. Study of strained engineer MOSFET and MOSFET compact models.

MODULE-I **10 hours**

History of device simulation, History of process simulation, Evolution of TCAD, Process flow integration, TCAD and compact model, Parameter extraction, TCAD for nanoelectronics, Modeling of Oxidation, Modeling of Diffusion,Modeling of Ion implantation, Modeling of Epitaxy and Lithography,Modeling of Etching and Deposition

MODULE-II10 hours

Synopsys TCAD Tools, SILVACO: TCAD simulation suite, Process-to-device simulation using SILVACO, Simulation example: strained-Si MOSFET,SOI MOSFET, SiGe, GaAs processing equipment MBE, RTCVD, UHV-CVD ,Various characterization tools like AUGER / ESCA, SIMS, RBS

MODULE-III10 hours

Strain-engineered MOSFETs- Scaling issues, Mobility-enhanced substrate engineering, Channel engineering, Gate engineering, Strained-engineered CMOS technology, Strain-engineered MOSFETs: simulation, Fabrication of SOI wafers, SOI devices, Double-gate MOSFET, TCAD simulation of SOI devices, Strained-Si MOSFETs on SOI, Modeling of multi-gate SOI devices

MODULE-IV10 hours

MOSFET compact models- Charge-based MOSFET models, Surface-potential based MOSFET models, Model evaluation, Modeling of SOI MOSFETs, Modeling of heterostructure MOSFETs, RF MOS modeling, Large-signal MOSFET models, Modeling of passive components- Inductor, Capacitor and Resistor

Text Book*s*

1. Semiconductor Devices: Physics and Technology – by S.M. Sze, John Wiley and Sons, 2nd edition, 2001.
2. TCAD for Si,SiGe and GaAS integrated circuits by G.A.Armstrong and C.K.Maiti,The Institution of Engineering and Technology,1st edition,2007
3. Fundamentals of Modern" VLSI Devices –by Y. Taur and T. H. Ning, 2nd edition, Cambridge University press, 1998.

COURSE OUTCOME:

1. Able to fabricate devices on TCAD.
2. Improve the MOSFET characteristics.

VLSI ALGORITHMS (3-1-0)

COURSE OBJECTIVE:

1. Study of VLSI automation algorithms.
2. Study of Global routing.
3. Study of cell routing & via minimization.

MODULE-I10 hours

VLSI Automation Algorithms: General Graph Theory and Basic VLSI Algorithms. Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing & Evolution, Other PartitioningAlgorithms.

MODULE-II 10 hours

Placement, floor planning & pin assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms formixed block & cell design. General & channel pin assignment.

MODULE-III 10 hours

Global Routing: Problem formulation, classification of global routing algorithms, Maze routingalgorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches. (6 lectures)

Detailed routing: problem formulation, classification of routing algorithms, single layer routingalgorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

MODULE-IV 10 hours

Over the cell routing & via minimization: two layers over the cell routers constrained & unconstrained via minimization.

Compaction: problem formulation, one-dimensional compaction, two dimension based compaction,hierarchical compaction.

Text Books

1. NaveedShervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher,
Second edition, 2005.
2. ChristophnMeinel& Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP,
2002.

Referance Books

1. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition, 2002
2. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

COURSE OUTCOME:

1. Able to formulate floor partitioning.
2. Able to implement multilayer routing.
3. Able to do perfect compaction.

VLSI DESIGNLABORATORY-I: (0-0-3) Credit: 2

(The Following Experiments Need to be Carried out Using Mentor Graphics and Cadence Digital and Analog Design Environments)

COURSE OBJECTIVE:

1. Aims at designing various analog & digital VLSI circuits.
2. Aims at familiarisation with various VLSI related software.

1. Design of different Current mirror circuits
2. Design of Reference Circuits
3. Design of Amplifiers
4. Design of Differential Amplifiers
5. Design of CMOS OP-AMP
6. Design of Comparators
7. Design of flash ADC
8. Design of SAR ADC
9. Design of Switch Capacitor Filter
10. Implementation of VCO by Ring Oscillator design
11. Design of DPLL
12. Design of ADPLL

COURSE OUTCOME:

1. Students can design current mirror, amplifiers, OPAMPs, etc. using software.
2. They can also analyzeADC, DAC, DPLL , etc.

VLSI TECHNOLOGYLABORATORY: (0-0-3) Credit: 2

COURSE OBJECTIVE:

1. Aims at studying various VLSI design processes using software.
2. Aims at familiarisation with various VLSI fabrication techniques.

1. Study of crystal growth and wafer Preparation
2. Study of Epitaxial Growth
3. Study of Oxidation
4. Study of Lithography
5. Study of Etching
6. Study of Deposition
7. Study of Diffusion
8. Study of Ion Implantation
9. Study of Metallization
10. Study of Packaging

COURSE OUTCOME:

1. Students can conceptualize the methods of wafer preparation, epitaxial growth, etc. .
2. They can also analyze various processes like ion implantation, metallization, etc.

HDL AND HIGH LEVEL VLSI DESIGN: (3-1-0) Credit: 4

COURSE OBJECTIVE:

1. This course is an introduction to the VHDL language. The emphasis is on writing synthesizable code and enough simulation code to write a viable test-bench. Structural, register transfer level (RTL), and behavioral coding styles are covered.
2. This class addresses targeting Xilinx devices specifically and FPGA devices in general.
3. The information gained can be applied to any digital design by using a top-down synthesis design approach.

MODULE-I **10 hours**

Basic Concepts of Hardware Description Languages., Hierarchy, Concurrency, Logic and Delay Modeling, Structural, Data-Flow and Behavioral Styles of Hardware Description, Architecture of Event Driven Simulators, Syntax and Semantics of VHDL, Variable and Signal Types, Arrays and Attributes, Operators, Expressions and Signal Assignments, Entities, Architecture Specification and Configurations, Component Instantiation, Concurrent and Sequential Constructs, Use of Procedures and Functions, Examples of Design Using VHDL, Synthesis of Logic From Hardware Description .

MODULE –II **10 hours**

Abstraction Levels in VLSI Design; Adder Architectures, Multiplier Architectures, Counter Architectures, ALU Architectures. Latches, Flip-Flops, Registers and Register Files. PLA Design, Gate Array Approach, Standard Cell Approach, PLA-Based Implementation, Random Logic Implementation, Micro-Programmed Implementation (ROM-Based Implementation).

MODULE –III10 hours

State machine: Introduction, Design style 1, Design style 2, Encoding style: Binary to OneHot, Moore machine, Mealy machine, String Detector, Traffic Light Controller.

MODULE –IV **10 hours**

SRAM Cell, Different DRAM Cells, Arraying of Cells, Address Decoding, Read / Write Circuitry, Sense Amplifier Design, ROM Design. Clock Skew, Clock, Distribution and Routing, Clock Buffering, Clock Domains, Gated Clock, Clock Tree, Concept of Logic Hazards.

Text Books

1. C. H. Roth, Digital Systems Design Using VHDL, Thomson Publications, Fourth Edition, 2002.
2. V. A. Pedroni, Circuit Design with VHDL, MIT Press/PHI, 2004.

Reference Books

1. Parhami, Behrooz, Computer Arithmetic: Algorithms and Hardware Designs, Oxford University Press, 2009.
2. Z. Navabi, Verilog Digital System Design, Second Edition, Tata McGrawHill, 2008.
3. R. C. Cofer and B. F. Harding, Rapid System Prototyping with FPGAs: Accelerating the Design Process, Elsevier/Newnes, 2005.

COURSE OUTCOME:

1. Implement the VHDL portion of coding for synthesis.
2. Identify the differences between behavioral and structural coding styles.
3. Understand the basic principle of circuit design and analysis.

VLSI SIGNAL PROCESSING :(3-1-0) Credit: 4

COURSE OBJECTIVE:

1. Introduce students to the fundamentals of VLSI signal processing and expose them to examples of applications.
2. Design and optimize VLSI architectures for basic DSP algorithms.
3. Design and optimize VLSI architectures for basic DSP algorithms.

MODULE-I **10 hours**

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

MODULE-II **10 hours**

Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.

MODULE-III **10 hours**

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

MODULE-IV **10 hours**

Fast Convolution: Introduction, Cook, Toom Algorithm, Winogard Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Text Books

1. Keshab K. Parhi. *VLSI Digital Signal Processing Systems*, Wiley-Inter Sciences, 1999
2. Mohammed Ismail, Terri, Fiez, *Analog VLSI Signal and Information Processing*, McGraw Hill, 1994.
3. Kung. S.Y., H.J. While house T.Kailath, *VLSI and Modern singal processing*, Prentice Hall, 1985.
4. Jose E. France, YannisTsividls, *Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing*' Prentice Hall, 1994.

COURSE OUTCOME:

1. Understand VLSI design methodology for signal processing systems.
2. Be familiar with VLSI algorithms and architectures for DSP.

3. Be able to implement basic architectures for DSP using CAD tools.

VLSI TESTING :(3-1-0) Credit: 4

COURSE OBJECTIVE:

1. This course covers introduction to the concepts and techniques of VLSI (Very Large Scale Integration) design verification and testing.
2. Details of test economy, fault modeling and simulation, defects, Automatic Test Pattern Generation (ATPG), design for testability, and built-in self-test (BIST) also covered.
3. To know about the various test Generation Algorithms and Fault Simulation Techniques.

MODULE-I 10 hours

Basics of Testing and Fault Modeling: Introduction, Principle of Testing, Types of Testing-DC and AC Parametric Tests, Fault Modeling-Stuck-At Faults-Fault Equivalence, Fault Collapsing, Fault Dominance, Fault Simulation.

MODULE-II10 hours

Testing of Combinational Circuits: Test Generation Basics, Test Generation Algorithms-Truth Table and Fault Matrices, Path Sensitization, Boolean Difference, D-Algorithm, PODEM, FAN, Delay Fault Detection. Testing of Sequential Circuits: Testing of Sequential Circuits as Iterative Combinational Circuits, State Table Verification, Test generation Based on Circuit Structure.

MODULE-III 10 hours

Design for Testability: Ad Hoc Techniques, Scan Path Technique, Level –Sensitive Scan Design, Random Access Scan Technique, Partial Scan, Non Scan Technique, Boundary Scan.

MODULE-IV10 hours

Built-in Self-Test: Test Pattern Generation for BIST-Exhaustive Testing, Pseudo exhaustive Pattern Generation, Pseudorandom Pattern Generator, Deterministic Testing.Output Response Analysis- Transition Count, Syndrome Checking, Signature Analysis, BIST Architecture-Built in Logic Observer, Self Testing Using an MISR and Parallel Shift Register Sequence Generator, LSSD on Chip Self Test.

Text Books

1. P.K.Lala, "*Digital Circuit Testing and Testability*", Academic Press, 2002

2. M.L.Bushnell & V.D.Agarwal, "*Essentials of Electronic Testing for Digital, Memory and Mixed signal VLSI Circuits"*,Kluwer Academic Publishers, 2004

Reference Books

1. N.K Jha and S.G Gupta ,"*Testing of Digital Systems*", Cambridge University Press, 2003.

2. Zainalabe Navabi, "*Digital System Test and Testable Design: Using HDL Model and Architecture"*, Springer,2010
3. Laung-Terng Wang,Cheng-Wen Wu,Xiaoqing Wen,VLSI '*Test Principles and Architectures*", Morgan Kaufmann Publishers, 2006

COURSE OUTCOME:

1. Apply the concepts in testing which can help them design a better yield in IC design.
2. Tackle the problems associated with testing of semiconductor circuits at earlier designlevels so as to significantly reduce the testing costs.

ELECTIVE – III/IV

DIGITAL SIGNAL PROCESSOR ARCHITECTURES (3-1-0) Credit: 4

COURSE OBJECTIVE:

1. The objective is to learn DSP Architecture, digital filters, power estimation technique in DSP, advanced architectures and processor of DSP.
2. To give an exposure to the various fixed point & a floating point DSP architectures and to develop applications using these processors.
3. To give students practice in applying DSP theory to real-world situations, and DSP programming experience.

MODULE-I **10 hours**

Introduction: A Digital Signal-Processing System, Analysis and Design Tool for DSP Systems, Computational Accuracy in DSP Implementations: Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementations, A/D Conversion Errors, DSP Computational Errors, D/A Conversion Errors.

MODULE-II **10 hours**

Architecturefor Programmable DSP Devices:Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Module, Programmability and Program Execution, Speed Issues, Features for External Interfacing, Execution Controland Pipelining: Hardware Looping, Interrupts, Stacks, Relative Branch Support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching Effects, Interrupt Effects, Pipeline Programming Models

MODULE-III **10 hours**

Programmable Digital Signal Processors: Commercial Digital Signal-Processing Devices, Data Addressing Modes of TMS320C54XX Processors, Memory Space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

MODULE-IV **10 hours**

The Q-Notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and Scaling, Bit- Reversed Index Generation, An 8-Point FFT Implementation on The TMS320C54XX, Computation of The Signal Spectrum.Memory Space Organization, External Bus Interfacing Signals, Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O, Direct Memory Access (DMA).A

Multichannel Buffered Serial Port (MCBSP), MCBSP Programming, A CODEC Interface Circuit, CODEC Programming, A CODEC-DSP Interface Example.

Text Books

1. Singh, A. and Srinivasan, S., "*Programmable DSP Architecture and Applications"*Thomson, 2004.
2. Lapsley, P. etal , "*DSP Processor Fundamentals: Architectures and Features*", IEEE Press, 1997
3. SenM.kuo, Woon-Seng S. Gan"Digital Signal Processors Architecture, Implementations and Applications", Pearson,2013

Referance Books

1. Bateman, A. and Yates, W. "*Digital Signal Processing Design"*, Computer Science Press, 1989.
2. Texas Instrument "*Digital Signal Processing Applications with the TMS320 Family*", Prentice-Hall, 1988.
3. Texas Instruments, "Linear Circuits: *Data Conversion, DSP Analog Interface, and Video Interface*", 1992.

COURSE OUTCOME:

1. Describe the specific architecture of the DSP processor used in this class, and understand the architecture of similar commercially produced DSP processors.
2. Discussvarious issues that need to be addressed when implementing DSP algorithms in real hardware with finite resources such as processing speed, memory, and bit resolution.
3. Write assembler code to implement basic DSP algorithms such as linear filtering with FIR and IIR filters.

DESIGN WITH ASICS :(3-1-0) Credit: 4

COURSE OBJECTIVE:

1. To introduce students to the process of designing application specific hardware implementations of algorithms for ASICs.
2. Students will work with commercial computer aided design tools to synthesize designs described in hardware description languages.
3. Topics covered will include differences between hardware description languages for synthesis and simulation, behavioral synthesis, gate-level design, register transfer level design, design methodologies, finite state machines, design reuse and intellectual property cores, and optimization.

MODULE-I 10 hours

Types of ASICs. ASIC Design Flow. Programmable ASICs. Anti Fuse, SRAM, EPROM, EEPROM Based ASICs. Programmable ASIC Logic Cells and I/O Cells. Programmable Interconnects. An Overview of Advanced FPGAs and Programmable SOCs: Architecture and Configuration of Spartan and Virtex FPGAs. Apex and Cyclone FPGAs. Virtex PRO Kits and Nios Kits. OMAP.

MODULE-II 10 hours

ASIC Physical Design Issues. System Partitioning, Interconnect Delay Models and Measurement of Delay. ASIC Floor Planning, Placement and Routing.

MODULE-III 10 hours

Design Issues in SOC. Design Methodologies. Processes and Flows. Embedded Software Development for SOC. Techniques for SOC Testing. Configurable SOC. Hardware/Software Co-design. High Performance Algorithms for ASICs/ SOCs.

MODULE-IV 10 hours

SOC Case Studies- DAA and Computation of FFT and DCT. High Performance Filters Using Delta-Sigma Modulators. Case Studies: Digital Camera, Bluetooth Radio/Modem, SDRAM and USB Controllers.

Text Book

1. M.J.S. Smith: *Application Specific Integrated Circuits,* Pearson, 2003

Reference Book

1. K.K.Parhi, *VLSI Digital Signal Processing Systems,* John-Wiley, 1999

COURSE OUTCOME:

2. Students will be able to design and synthesize a complex digital functional block, containing over 1,000 gates, using Verilog HDL.
3. Students will demonstrate an understanding of how to optimize the performance, area, and power of a complex digital functional block, and the tradeoffs between these.
4. Students will demonstrate an understanding of issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design.

MEMS AND IC DESIGN :(3-1-0) Credit: 4

COURSE OBJECTIVE:

1. Introduction to MEMS and micro fabrication.
2. To study various sensing and transduction technique.
3. To know various fabrication and machining process of MEMS.

MODULE-I 10 hours

Overview of CMOS Process in IC Fabrication, MEMS System-Level Design Methodology, Equivalent Circuit Representation of MEMS, Signal-Conditioning Circuits, and Sensor Noise Calculation.

MODULE-II 10 hours

Pressure Sensors with Embedded Electronics (Analog/Mixed Signal): Accelerometer with Transducer, Gyroscope, RF MEMS Switch with Electronics, Bolo Meter Design.

MODULE-III 10 hours

RF MEMS

MODULE-IV 10 hours

Optical MEMS

Text Books

1. Gregory T.A. Kovacs, *Micromachined Transducers Sourecbook*, McGraw-Hill Inc., 1998
2. Stephen D. Senturia, *Microsystem Design*, Kluar Publishers, 2001
3. NadimMaluf, *an Introduction to Microelectromechanical Systems Engineering*, Artech House, 2000
4. M.H. Bao, *Micro Mechanical Transducers*, Volume 8, Handbook of Sensors and Actuators, Elsevier, 2000
5. Masood Tabib-Azar, *Microactuators*, Kluwer, 1998
6. LjubisaRistic, Editor, *Sensor Technology and Devices*, Artech House, 1994
7. D. S. Ballantine, et. al., *Acoustic Wave Sensors*, Academic Press, 1997
8. H. J. De Los Santos, *Introduction to Microelectromechanical (MEM) Microwave Systems*, Artech, 1999
9. James M.Gere and Stephen P. Timoshenko, *Mechanics of Materials*, 2nd Edition, Brooks/Cole Engineering Division, 1984

COURSE OUTCOME:

1. Be familiar with the important concepts applicable to MEMS, their fabrication.
2. Be fluent with the design, analysis and testing of MEMS.
3. Apply the MEMS for different applications.

PHYSICAL DESIGN AUTOMATION :(3-1-0) Credit: 4

COURSE OBJECTIVE:

1. This course focuses on various design automation problems in the physical design process of VLSI circuits, including: logic partitioning, floorplanning, placement, global routing, detailed routing, clock and power routing, and new trends in physical design.
2. To impart knowledge on implementation of graph theory in VLSI.
3. To impart knowledge on automation methods for VLSI physical design.

MODULE-I 10hours Preliminaries: Introduction to Design Methodologies, Design Automation Tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems. General purpose methods for combinational optimization: Backtracking, Branch And Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms.

MODULE-II 10 hours

Layout Compaction, Placement, Floor Planning And Routing Problems, Concepts and Algorithms. Modeling and simulation: Gate Level Modeling and Simulation, Switch Level Modeling and Simulation.

MODULE-III 10 hours

Logic synthesis and verification: Basic Issues and Terminology, Binary-Decision Diagrams, Two-Level Logic Synthesis. High-level synthesis: Hardware Models, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some Aspects of Assignment Problem, High-Level Transformations.

MODULE-IV 10 hours

Physical design automation of FPGA‟ S: FPGA Technologies, Physical Design Cycle for FPGA‟ s, Partitioning and Routing for Segmented and Staggered Models. Physical design automation of MCM‟ S: MCM Technologies, MCM Physical Design Cycle, Partitioning, Placement - Chip Array Based And Full Custom Approaches, Routing – Maze Routing, Multiple Stage Routing, Topologic Routing, Integrated Pin –Distribution And Routing, Routing And Programmable MCM‟ s.

Text Books

1. NAVEED SHEWANI, "*Algorithms for VLSI Physical Design Automation*", Kluwer Academic, 1993
2. S.H. Gerez, "*Algorithms for VLSI Design Automation*", John Wiley, 1998.
3. S.M. Sait& H. Youssef, "*VLSI Physical Design Automation*", World scientific, 1999.
4. M.Sarrafzadeh, "*Introduction to VLSI Physical Design*", McGraw Hill (IE), 1996

COURSE OUTCOME:

1. Students are able to know how to place the blocks and how to partition the blocks while for designing the layout for IC.
2. Students are able to analyze physical design problems and Employ appropriate automation algorithms for partitioning, floor planning, placement and routing.
3. Students are able to decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing.

CMOS RF CIRCUIT DESIGN (3-1-0)

COURSE OBJECTIVE:

1. To educate students fundamental RF circuit and system design skills.
2. To introduce students, the basic RF electronics utilized in the industry and how to build up a complex RF system from basis.
3. To offer students experience on designing and simulating RF circuits in computer.

MODULE-I 08hours

Introduction, Basic concepts in RF Design, Passive RLC networks, Passive IC components

MODULE-II 12hours

High frequency amplifier design, Voltage references & biasing, LNA design, Mixers

MODULE-III 12hours

RF power amplifier, PLL, Oscillators, Synthesizers

MODULE-IV 08hours

Noise, Phase noise, Feedback systems

Text Books

1. The Design of CMOS RF Integrated Circuits, By T. H. Lee, Cambridge University Press
2. RF Microelectronics, By B. Razavi, Pearson

COURSE OUTCOME:

1. Ability to design and conduct simulations and experiments.
2. Ability to design a system, component or process to meet desired needs.
3. Become proficient with computer skills (eg., Multisim, HSPICE, Virtuoso) for the analysis and design of circuits.

EMBEDDED SYSTEM DESIGN :(3-1-0) Credit: 4

COURSE OBJECTIVE:-

1. Students have knowledge about the basic functions of embedded systems.
2. Students have knowledge about the applications of embedded systems.
3. Students have knowledge about the development of embedded software.

MODULE-I 10 hours

Introduction: An Embedded System, Processor in The System, Other Hardware MODULEs, Software Embedded into a System, Exemplary Embedded Systems, Embedded System-On-Chip (SOC) and in VLSI Circuit. Devices and Device Drivers: I/O Devices, Timer and Counting Devices, Serial Communication Using The „I2C‟, „CAN‟ and Advanced I/O Buses between the Networked Multiple Devices, Host System or Computer Parallel Communication between the Networked I/O Multiple Devices Using the ISA, PCI, PCI-X and Advanced Buses, Device Drivers, Parallel Port Device Drivers in a System, Serial Port Device Drivers in a System, Interrupt Servicing (Handling) Mechanism.

MODULE-II 10 hours

Software and Programming Concept: Processor Selection for an Embedded System, Memory Selection for an Embedded System, Embedded Programming in C++, Embedded Programming in Java, Unified Modelling Language (UML), Multiple Processes and Application, Problem of Sharing Data by Multiple Tasks and Routines, Inter Process Communication.

MODULE-III 10 hours

Real Time Operating System: Operating System Services, I/O Subsystems, Network Operating Systems, Real-Time and Embedded System Operating Systems, Need of a Well Tested and Debugged Real-Time Operating System (RTOS), Introduction to Mc/OS-II. Case Studies of Programming with RTOS: Case Study of an Embedded System for a Smart Card.

MODULE-IV 10 hours

Hardware and Software Co-Design: Embedded System Project Management Embedded System Design and Co-Design Issues in System Development Process, Design Cycle in the Development Phase for an Embedded System, Use of Software Tools for Development of Embedded System, Issues in Embedded System Design.

Text Books

1. Ralf Niemann, Kluwer Academic, *Hardware Software Co-design of Embedded Systems,*
2. Hermann Kopetz, Kluwer Academic, *Design Principles of Distributed Embedded Applications,*
3. Sriram V. Iyer&Pankaj Gupta, *Embedded Real-Time Systems Programming,* TMH.

Referance Books

1. Peter Marwedel*Embedded System Design,* Springer, 2003
2. Wolf, *Embedded System Design,*

COURSE OUTCOME:-

1. Able to present the mathematical model of the system.
2. Able to develop real-time algorithm for task scheduling.
3. Able to work on design and development of protocols related to real-time communication.

LOW POWER VLSI DESIGN :(3-1-0) Credit: 4

COURSE OBJECTIVE:-

1. This course addresses a profound analysis on the development of the CMOS & Bi-CMOS digital circuits for a low voltage low power environment.
2. To study the concepts of device behavior and modelling.
3. To study the concepts of low voltage, low power logic circuits.

MODULE-I 10 hours

Introduction: Need for Low Power VLSI Chips, Sources of Power Dissipation on Digital Integrated Circuits. Emerging Low Power Approaches, Physics of Power Dissipation in CMOS Devices. Device & Technology Impact on Low Power: Dynamic Dissipation in CMOS, Transistor Sizing & Gate Oxide Thickness and Impact of Technology Scaling, Technology & Device Innovation. Power Estimation, Simulation Power Analysis: SPICE Circuit Simulators, Gate Level Logic Simulation, Capacitive Power Estimation, Static State Power, Gate Level Capacitance Estimation, Architecture Level Analysis, Data Correlation Analysis in DSP Systems, Monte Carlo Simulation. Probabilistic Power Analysis: Random Logic Signals, Probability & Frequency, Probabilistic Power Analysis Techniques, Signal Entropy.

MODULE-II 10 hours

Low Power Design: Circuit Level; Power Consumption in Circuits. Flip Flops & Latches Design, High Capacitance Nodes, Low Power Digital Cells Library. Logic Level; Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Pre-Computation Logic.

MODULE-III 10 hours

Low Power Architecture & Systems: Power & Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, Flow Graph Transformation, Low Power Arithmetic Components, Low Power Memory Design. Low Power Clock Distribution: Power Dissipation in Clock Distribution, Single Driver Vs Distributed Buffers, Zero Skew Vs Tolerable Skew, Chip & Package Co Design of Clock Network.

MODULE-IV 10 hours

Algorithm & Architectural Level Methodologies: Introduction, Design Flow, Algorithmic Level Analysis & Optimization, Architectural Level Estimation & Synthesis.

Text Books

1. Gary K. Yeap, *Practical Low Power Digital VLSI Design,* KAP, 2002
2. Kaushik Roy, Sharat Prasad, *Low-Power CMOS VLSI Circuit Design,* Wiley, 2000

Reference Books

1. Rabaey, Pedram, *Low power design methodologies,* Kluwer Academic, 1997
2. W. Nebel and J. Mermet, *Low Power Design in Deep Sub-micron Electronics,* Kluwer Academic Publishers, 1997

COURSE OUTCOME:-

1. Capability to recognize advanced issues in VLSI systems, specific to the deep-submicron silicon technologies.
2. Students able to understand deep submicron CMOS technology and digital CMOS design styles.
3. To design chips used for battery-powered systems and high performance circuits.

SYSTEM ON CHIP (SoC) DESIGN

COURSE OBJECTIVE:-

1. Understand What SoC is and what the differences between SoC and Embedded System.
2. Learn to employ specialized knowledge of subsystems like processor cores and other SoC components to design an embedded SoC.
3. Improve students' capabilities of using the technical knowledge of processor architecture, peripherals, programming, and CAD tools to design SoCs.

MODULE-I10 hours

Low-level modelling and design refactoring: Verilog RTL Design .Simulation styles (fluid flow versus eventing). Basic RTL to gates synthesis algorithm. Using signals, variables and transactions for component inter-communication. SystemC overview. Structural hazards, retiming, refactoring.

MODULE-II10 hours

Design partition, high-level and hybrid modelling: Bus and cache structures, DRAM interface. SoC parts. Design exploration. Hardware/software interfaces and co-design. Memory maps. Programmer's model. Firmware development.

MODULE-III10 hours

Transactional modelling. Electronic systems level (ESL). IP-XACT. Instruction set simulators, cache modelling and hybrid models. Assertions for design, testing and synthesis: Assertion based design: testing and synthesis.

MODULE-IV10 hours

PSL/SVA assertions. Temporal logic compilation to FSM. Glue logic synthesis. Combinational and sequential equivalence. High- level Synthesis and Automated Assembly. Power control and power modelling: Power consumption formulae. Pre-layout wiringestimates. Clock gating. Frequency and voltage dynamic scaling.

Text Books

1.Ghenassia, F. (2010). *Transaction-level modeling with SystemC: TLM concepts and applications for embedded systems*. Springer.
2.Grotker, T., Liao, S., Martin, G. & Swan, S. (2002). *System design with SystemC*. Springer.
3. OSCI. *SystemC tutorials and whitepapers*
4. Lin, Y-L.S. (ed.) (2006). *Essential issues in SOC design: designing complex systems-on-chip*.Springer.

COURSE OUTCOME: -

1. Able to design and develop embedded systems (hardware, peripherals and firmware).
2. Able to demonstrate embedded system applications.
3. Possess analytical and problem solving skills.

VLSI DESIGN LABORATORY-II: (0-0-3) Credit: 2

COURSE OBJECTIVE:

1. Students will be familiar withdigital VLSI circuits using software.
2. They can also analyze various types of VLSI modelling techniques.

(The Following Experiments Need to be Carried out Using HDL Simulation Tools)

1. Design a full adder using dataflow modelling.
2. Design a full adder using half-adder.
3. Design a half adder.
4. Design a 4-bit adder -cum-sub tractor using:

4:1 MUX using the following:

(a) Dataflow

(b) Using when else

(c) Structural modelling using 2:1 MUX

(d) Behavioural modelling using

(i) Case statement

(ii) If else statement

(e) Mixed style of modelling (use structural, behavioural, dataflow)

5. Design a decoder (3: 8) and Encoder (Gray to Binary).
6. Design a BCD to 7-Segment Decoder.
7. Interface the 2-bit adder with 7-segment display.
8. Design 4-bit Even/Odd parity checker & generator.
9. Design of Flip-Flops:

(a) S-R Flip Flop (b) J-K Flip Flop (c) D Flip Flop (d) T Flip Flop

10. (a) Design of counters:

(i) 4-bit up counter (use asynchronous reset)

(ii) 4-bit down counter (use synchronous reset)

(iii) 4-bit up/down counters

(iv) Decade Counter

(b) Design of Shift Registers:

(i) Serial-in serial-out

(ii) Serial-in parallel-out

(c) Design the following using Generics

(i) Generic Decoder

(ii) Generic Parity

(iii)Detector Generic parity generator

11. Design of a simple Microprocessor Data Path and Control Path using VHDL modelling

COURSE OUTCOME:

1. Students can design encoder, decoder, parity generator, etc. using software.
2. They can also analyze counters, flip flops, data path, etc.

ADVANCED SIMULATION LABORATORY: (0-0-3) Credit: 2

(The following experiments need to be carried out using MATLAB)

COURSE OBJECTIVE:

1. Students will study advanced simulation methods.
2. They can also analyze Higher Order Statistics.

1. Signal Decomposition using Multi Resolution Techniques.
2. Wavelet Coding Techniques
3. Spectral Estimation Using Parametric Method
4. Higher Order Statistics of a Signal
5. PCA/ICA Analysis

COURSE OUTCOME:

1. Students can conceptualize multi resolution techniques using MATLAB software.
2. They can also analyze spectral estimation methods along with PCA/ICA analysis..